CVxxx Series Single and Dual-Branch Downconverter Device Junction Temperatures vs. PCB Mounting Configuration

Introduction

This study investigated three PCB mounting configurations for WJ's CV-series products, and the resultant junction temperatures for the two active devices (die) contained therein. The CV products are packaged in a JEDEC standard 28-lead QFN 6 x 6 mm package. Multiple die are mounted and wire bonded to a copper leadframe, which is then encapsulated. The exposed leadframe bottom side is the intended thermal path to the PCB.

To maximize thermal dissipation, WJ recommends a PCB land pattern with 33 vias directly under the package, connected to backside and internal copper ground layers. In addition to multiple 1-oz copper layers (1.4-mils thick), it is recommended the vias utilize a .0135" diameter drill hole plated to a final diameter of .010". Figure 1 illustrates the mounting configuration including device, leadframe and PCB.

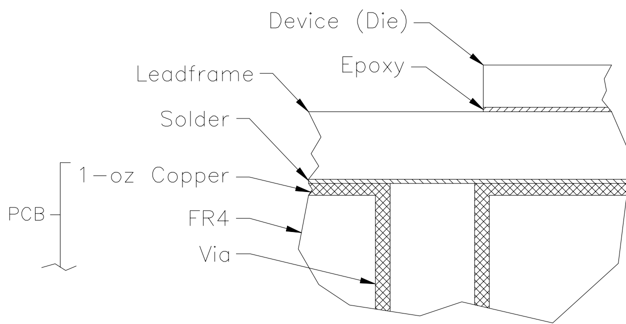

Figure 1: Mounting Configuration Cross-Section (molding compound not shown)

This study investigated two additional mounting configurations: twelve (12) vias and no vias under the package. These three configurations are illustrated in Figure 2.

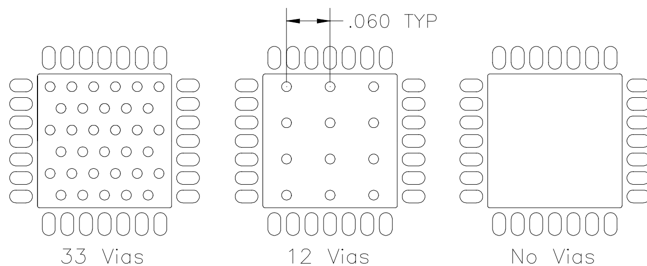

Figure 2: Via Configurations

Finite element models were generated for the 3 via configurations illustrated in Figure 2. Power was deposited over a region on top of the 2 active die corresponding to their respective heat generating areas. The models were not created to show fine detail of the die structure, but instead, to illustrate the heat flow below the active regions. The epoxy joint below each die and the leadframe depict dimensionally accurate models. The RF leads do not contribute to thermal spreading and were omitted for simplicity. The .063" thick FR4 PCB was modeled using four 1-ounce copper layers (top side, back side, 2 inner). In each of the 3 studies, boundary conditions were set with power deposition over active regions of the die, and backside PCB layer held at 0°C. The model is shown in Figure 3 (note: symmetry allows a half-model to be used).

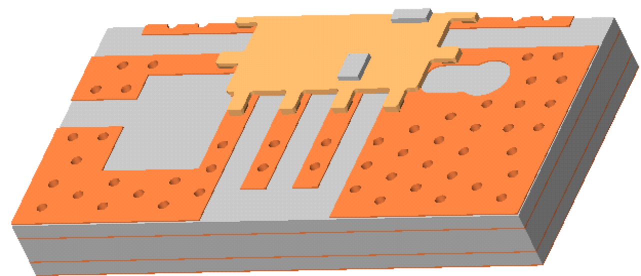

Figure 3: Finite Element Model showing die, leadframe and PCB construction (half-model; RF leads omitted)

Results

Thermal analyses were performed for each of the 3 studies, and temperature plots recorded. These plots are shown in the following Figures 4, 5 and 6.

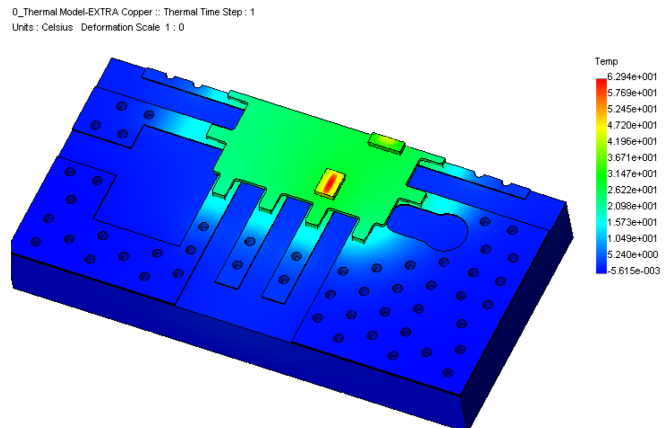

Figure 4: "No Vias" temperature profile of 2 active die; half model (scale is ^{o}C)

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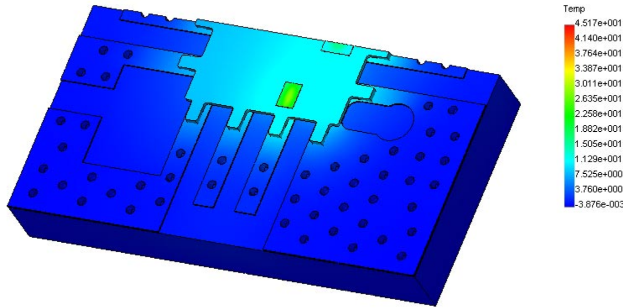

Figure 5: "12 Vias" temperature profile of 2 active die; half model (scale is °C)

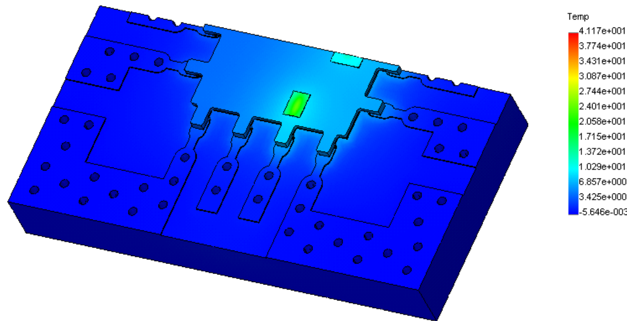

Figure 6: "33 Vias" temperature profile of 2 active die; half model (scale is °C)

The 3 studies are summarized in Table A. Overall thermal impedances (θ_{total}) listed in Table A are the sum of 2 values: (θ_1) the thermal impedance between the die junctions and backside of the attach material, and (θ_2) the thermal impedance between the backside of the attach material and the backside of the PCB. These two thermal paths are illustrated in Figure 7.

Table 1 shows expected junction temperatures for the different mounting configurations as a function of various PCB temperatures (85° C, 95° C and 105° C) for the CV2xx dual-branch downconverters. Table 2 shows the same information for the CV1xx single-branch downconverters. The additional RF amplifier in the single-branch downconverters is manufactured with the same process technology and thermal characteristics as the IF amplifier.

Note that for a minimum MTTF of $1x10^6$ hours, WJ specifies a maximum junction temperature (T_j) of 160° C for these devices. As expected, if the device is mounted using the WJ recommended configuration (33 vias), the device junction temperatures will be lower than the WJ recommended value up to a board temperature of 105° C. The second mounting option (12 vias) will allow operation below T_j = 160° C with a board temperature up to approximately 100° C. Finally, the "No Via" option is only viable up to a board temperature of 85° C leaving very little margin with this mounting option.

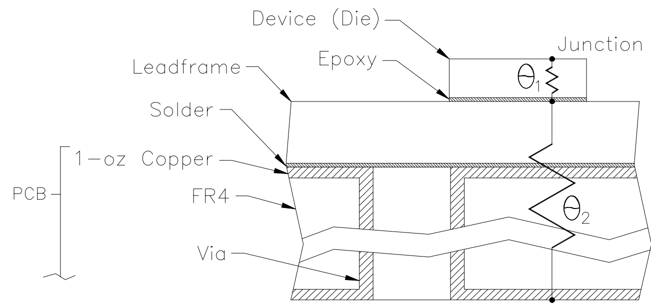

Figure 7: Thermal Impedance Paths

Study	IF Amplifier						LO Amplifier					
	Θ_1 (°C/W)	Θ_2 (°C/W)	Θ_{total} (°C/W)	Tj at PCB Backside 85° C	95° C	105° C	Θ_1 (°C/W)	Θ_2 (°C/W)	Θ_{total} (°C/W)	Tj at PCB Backside 85° C	95° C	105° C
With vias (qty. 33)	59	11.1	70.1	141	151	161	103.9	18.5	122.4	132	142	152
With vias (qty. 33)	59	16.1	75.1	145	155	165	103.9	28.9	132.8	136	146	156
No vias	59	38.3	97.3	163	173	183	103.9	75.8	179.7	154	164	174

Table 1: Data Summary – Junction Temperature (Tj) vs. Various PCB Backside Temperatures for CV2xx devices

Study	IF or RF Amplifier						LO Amplifier					
	Θ_1 (°C/W)	Θ_2 (°C/W)	Θ_{total} (°C/W)	Tj at PCB Backside 85° C	95° C	105° C	Θ_1 (°C/W)	Θ_2 (°C/W)	Θ_{total} (°C/W)	Tj at PCB Backside 85° C	95° C	105° C
With vias (qty. 33)	59	11.1	70.1	141	151	161	103.9	18.5	122.4	120	130	140
With vias (qty. 33)	59	16.1	75.1	145	155	165	103.9	28.9	132.8	123	133	143
No vias	59	38.3	97.3	163	173	183	103.9	75.8	179.7	136	146	156

Table 2: Data Summary – Junction Temperature (Tj) vs. Various PCB Backside Temperatures for CV1xx devices

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